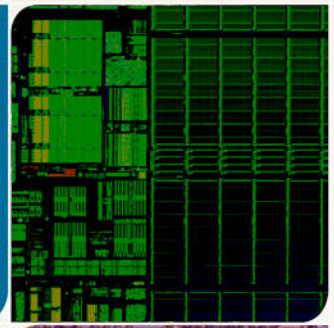
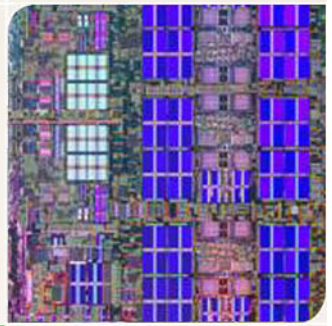
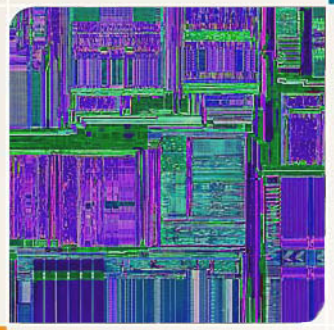
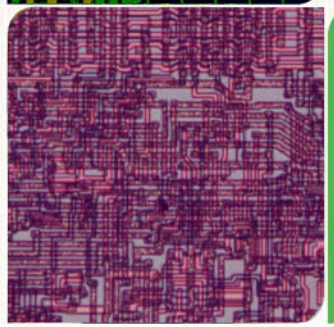
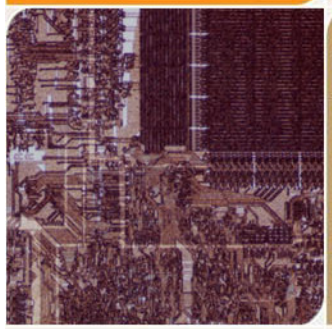



CS4803DGC Design Game Consoles

Spring 2009

Prof. Hyesoon Kim




Real-time Rendering Ch 18

Georgia Tech College of Computing

Mip Mapping

1024x1024

512x512

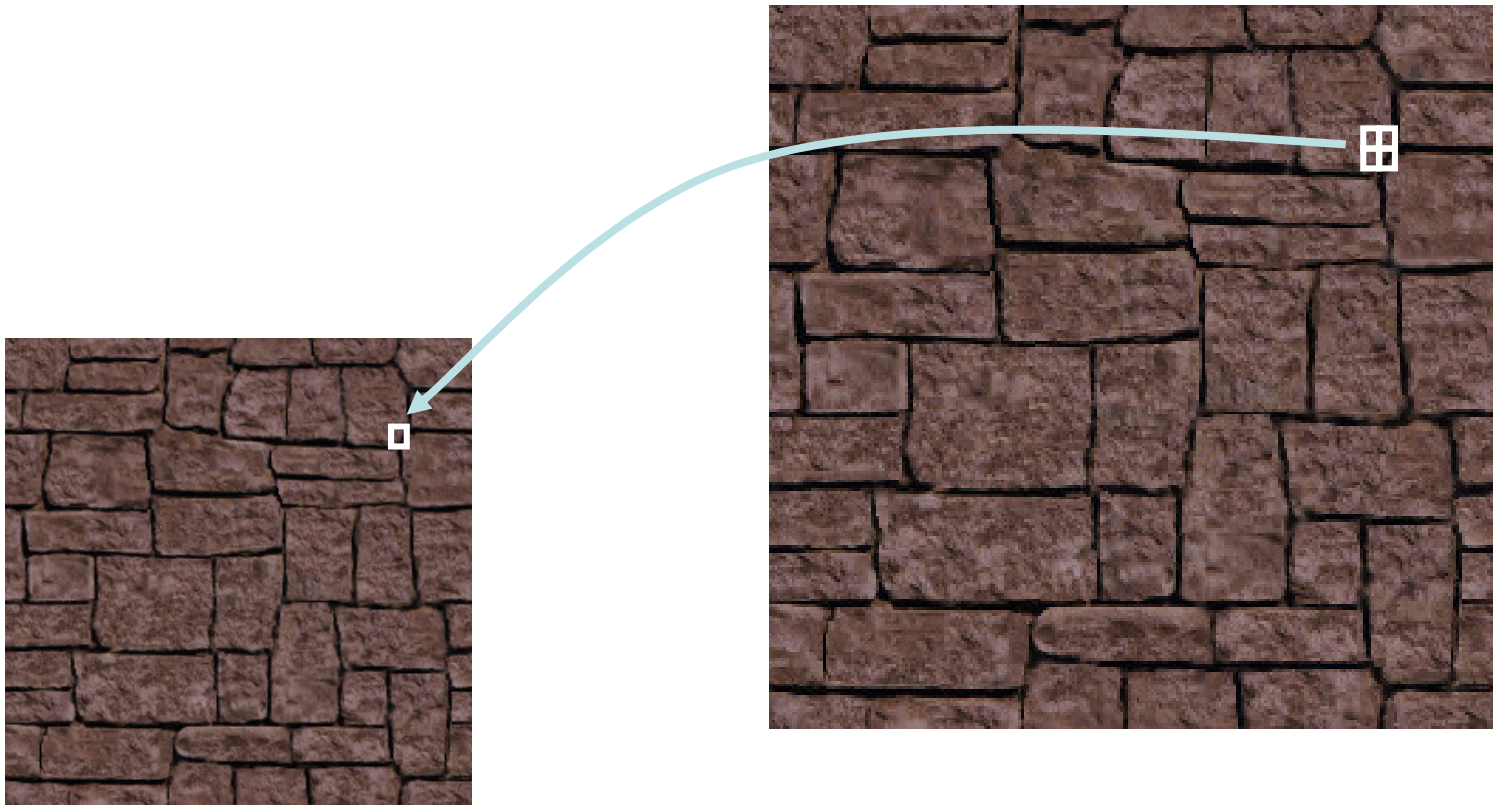
256x256

128x128

64x64



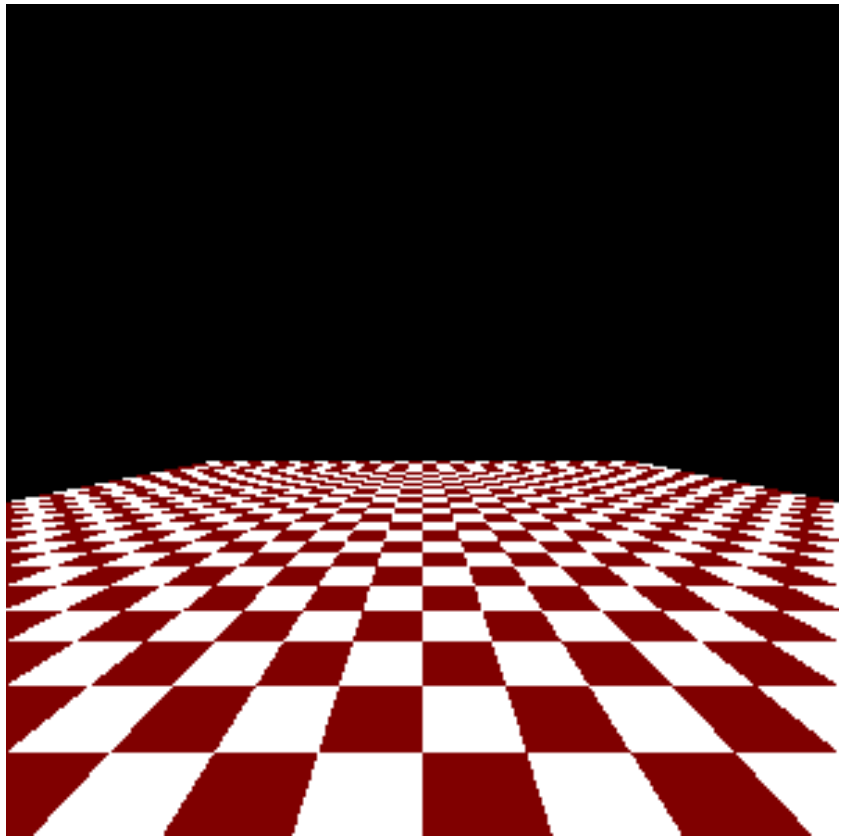
Bilinear Filtering



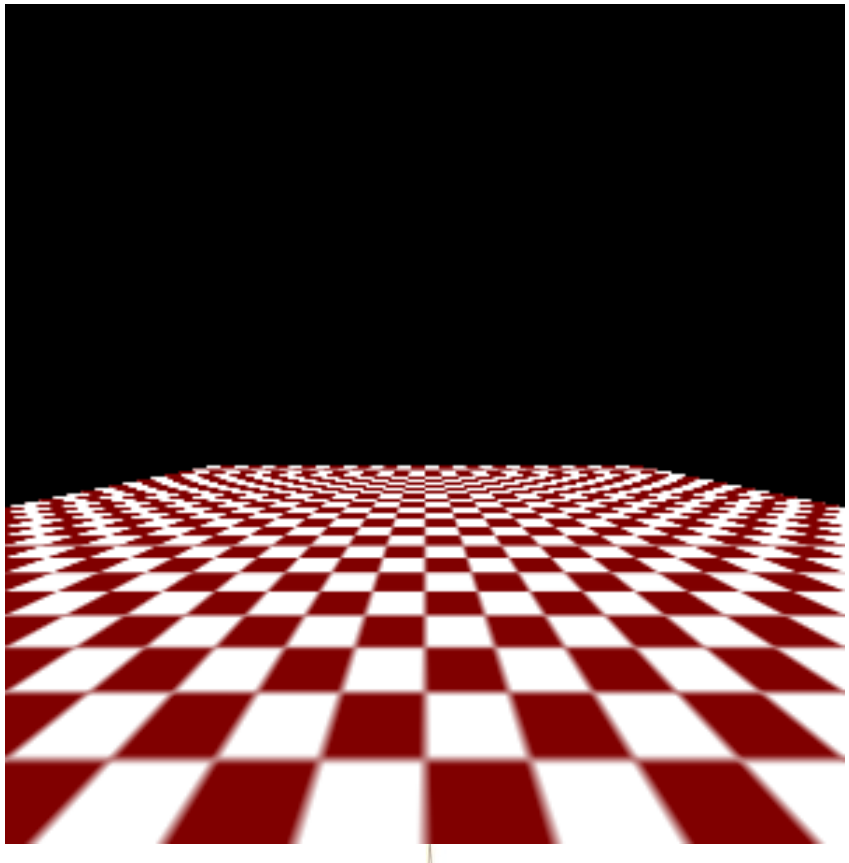


Texture Filtering - Good

Nearest



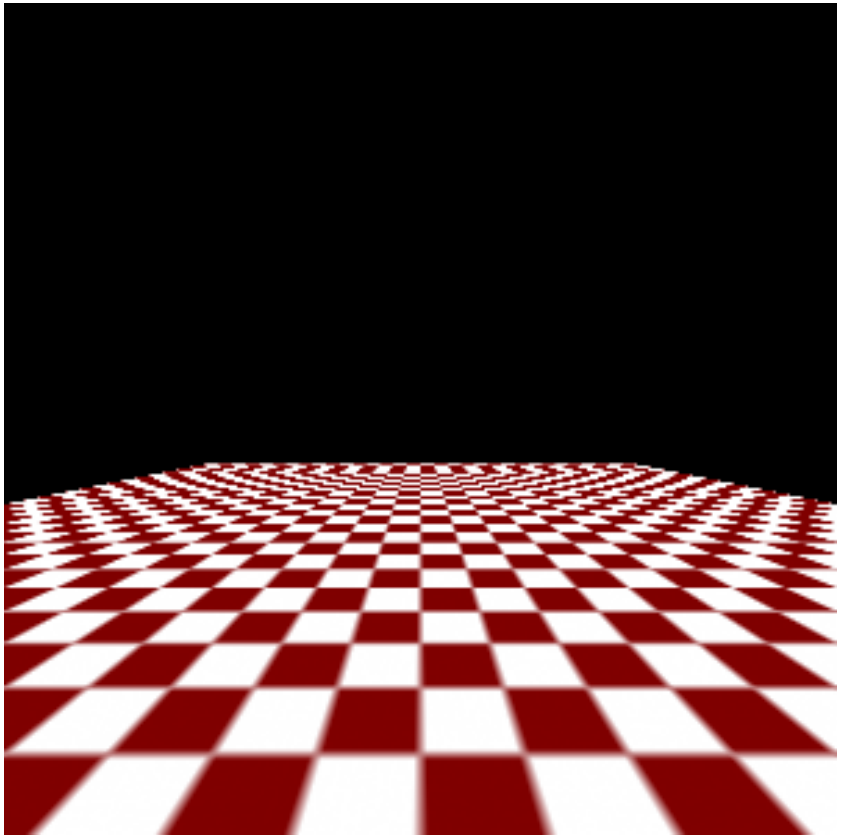
Bilinear



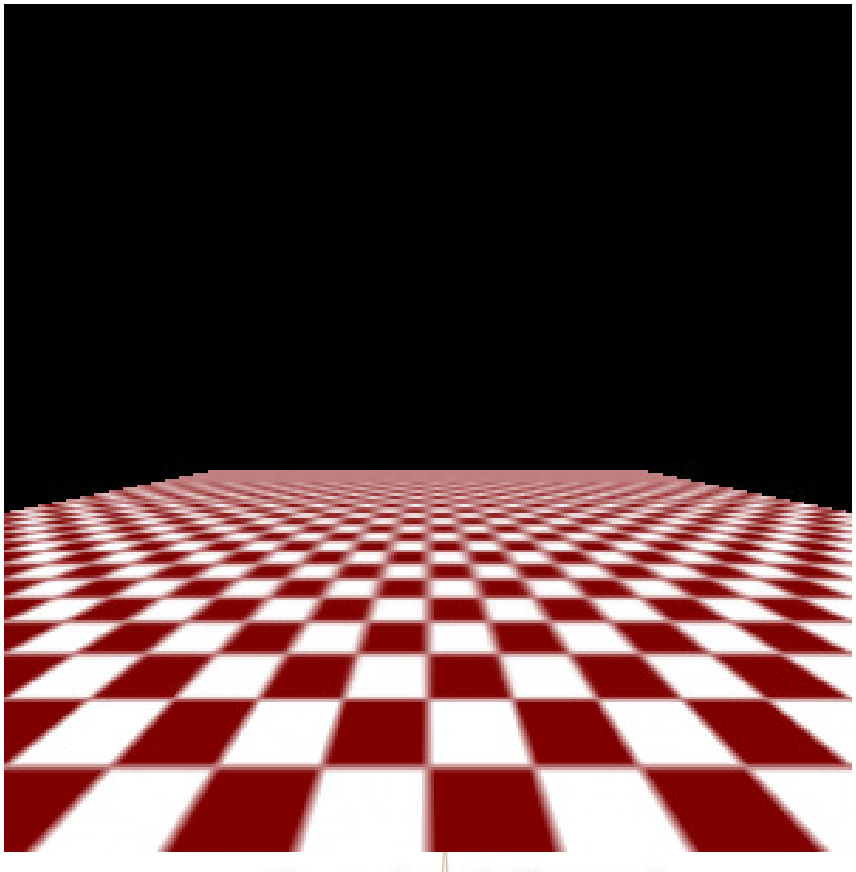


Texture Filtering - Better

Bilinear

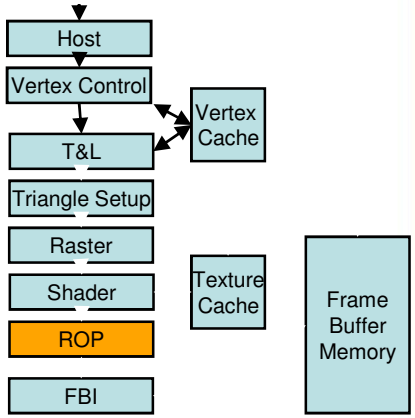


Trilinear



ROP (from Raster Operations)

- C-ROP performs frame buffer blending
  - Combinations of colors and transparency
  - Antialiasing
  - Read/Modify/Write the Color Buffer
- Z-ROP performs the Z operations
  - Determine the visible pixels
  - Discard the occluded pixels
  - Read/Modify/Write the Z-Buffer
- ROP on GeForce also performs
  - “Coalescing” of transactions
  - Z-Buffer compression/decompression



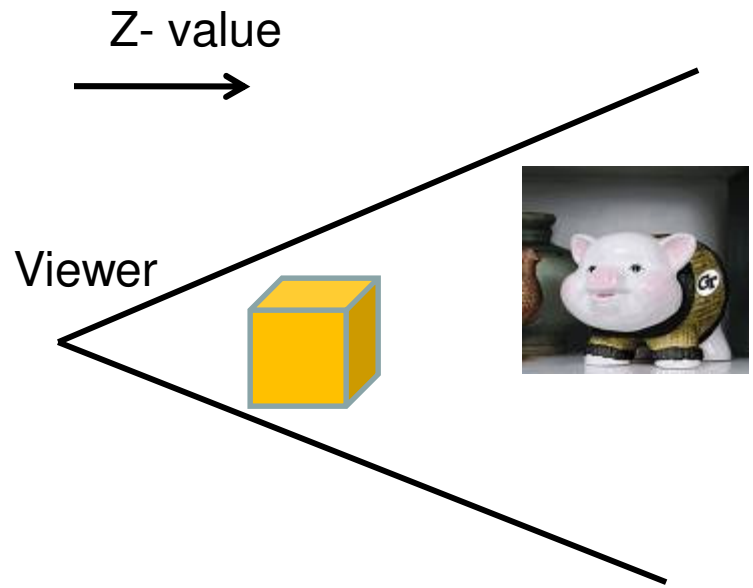
Review: The RASTERIZER
Z-buffering



- The Z-buffer (aka depth buffer)
- Idea:
  - Store z (depth) at each pixel
  - When scan-converting a triangle, compute z at each pixel on triangle
  - Compare triangle's z to Z-buffer z-value
  - If triangle's z is smaller, then replace Z-buffer and color buffer
  - Else do nothing
- Can render in any order

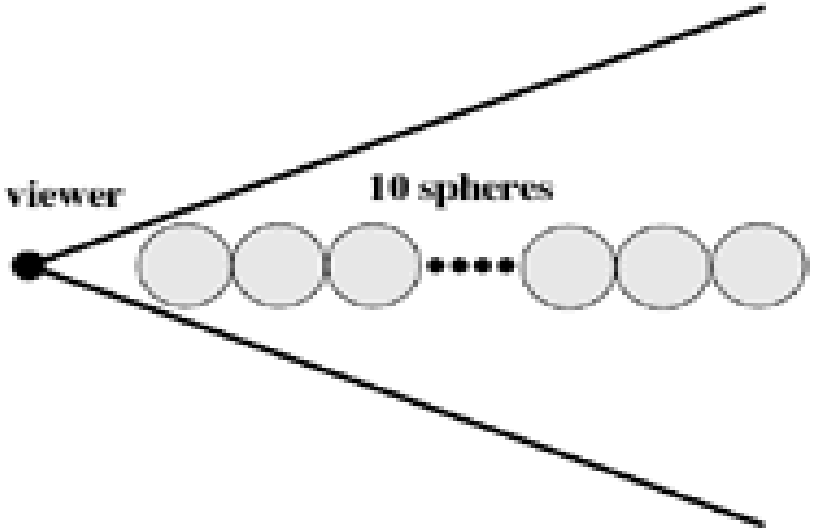
Z-value

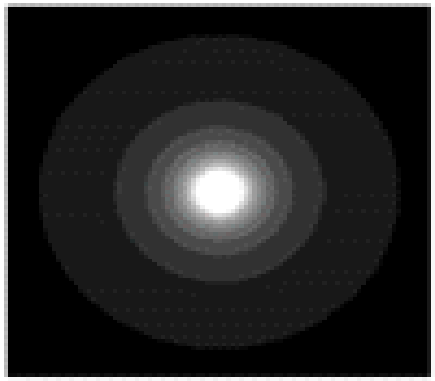
Z-value: distance from the viewer



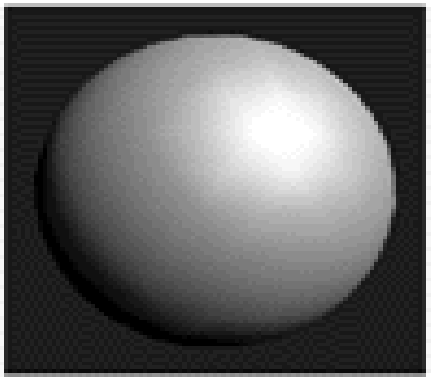
Occlusion Culling

- Cull: “select from a flock”, hiding surface for a performance
- Z-buffer is not smart enough





depth complexity



rendered image

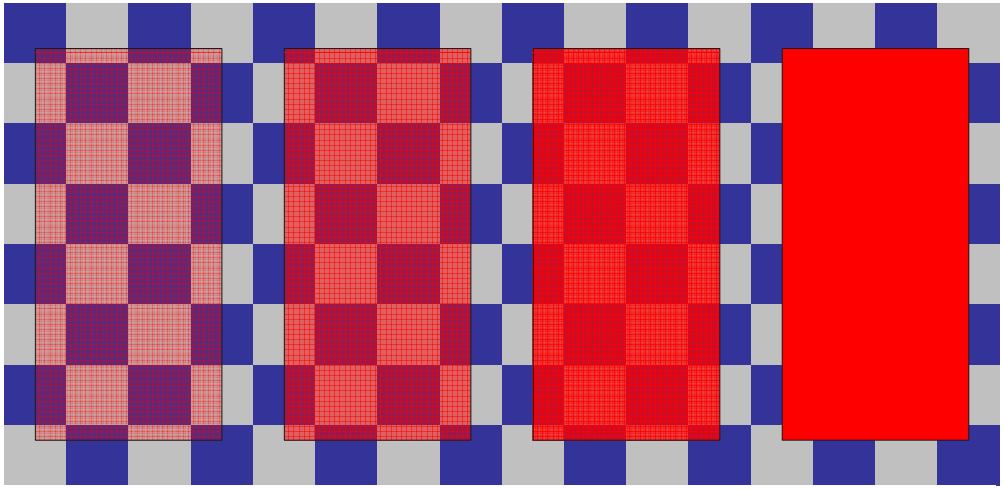
Eventually only one sphere is visible
Visibility check in an object level.

http://www.gamasutra.com/features/19991109/moller_haines_01.htm



Alpha Blending

- *Alpha Blending* is used to render translucent objects.
- The pixel's alpha component contains its *opacity*.
- Read-modify-write operation to the color framebuffer
- Result = alpha * Src + (1-alpha) * Dst

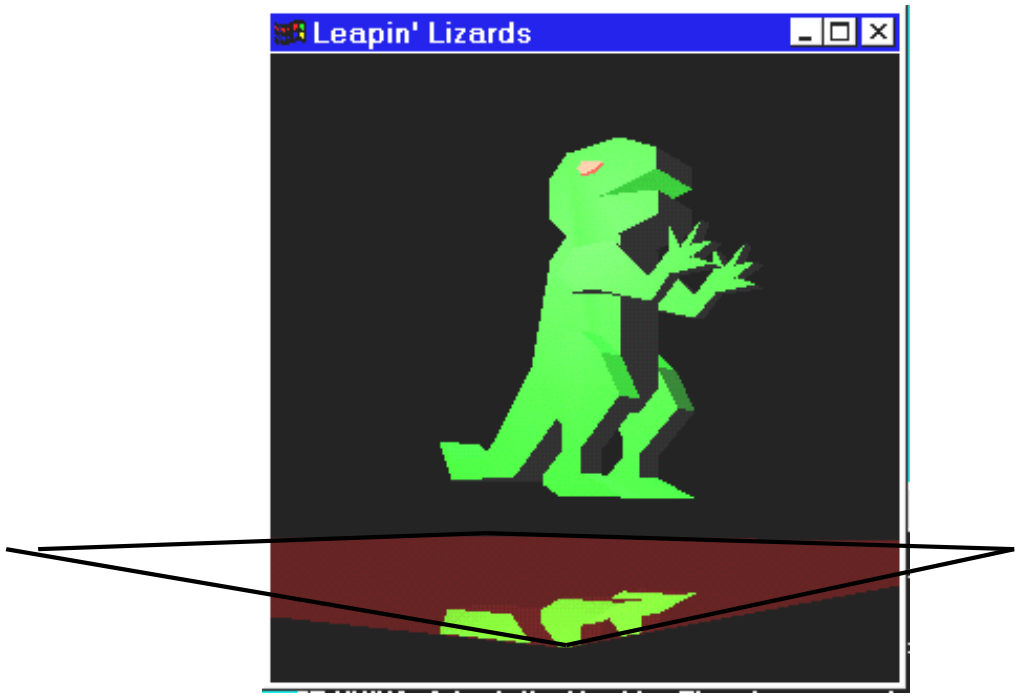




Stencil Buffer

- Per pixel operation
- Compares reference value to pixel's stencil buffer value
- Same spatial resolution as color and depth buffers
- Usually 8-bits'
- Used to hold vales related to elements being written into frame buffer

Stencil Maintains the Floor



Clear stencil to zero.
Draw floor polygon with stencil set to one.
Only draw reflection where stencil is one.



Buffers

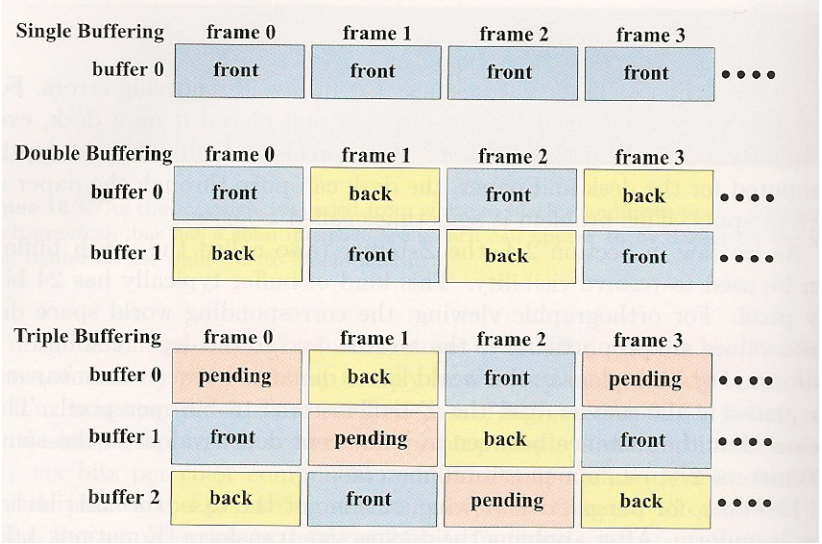
- Per pixel comparisons: Hardware is easy
- Z-buffer, Stencil buffer, Alpha values

- Xbox360 eDRAM performs these operations



Frame Buffers

- Color buffer is a part of the frame buffer
- Buffer->video controller->monitor
- Video Controller
  - Scan through the color buffer, scaline by scaline at the same rate as the monitor
  - Synchronization with the beam of the monitor
    - Electron beam: left-to-right, up-to-down



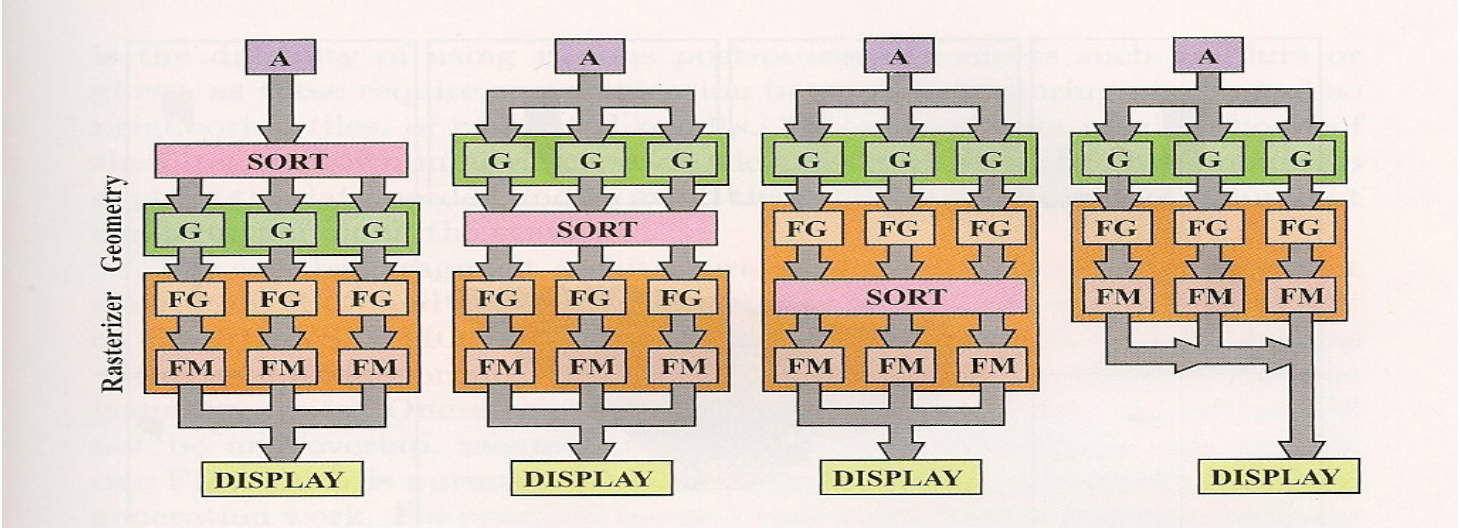


CPU vs GPU

- GPU
  - Many pipeline stages (400-600 stages)
  - Massive data parallelism
  - Memory access patterns are regular

Taxonomy of Parallel Graphics Architectures

- Sort-first, sort-middle, sort-last fragment, sort-last image
- FG: Fragment generation
  - The actual locations inside a primitive
- FM: Fragment merge
  - Merge the results using Z-buffer



Memory Architecture

- Xbox: unified memory architecture
- Xbox 360: hybrid
  - CPU and GPU share the same bus and interface to the system memory (texture memory)
  - GPU-exclusive memory
- Playstation3: GPU dedicated memory

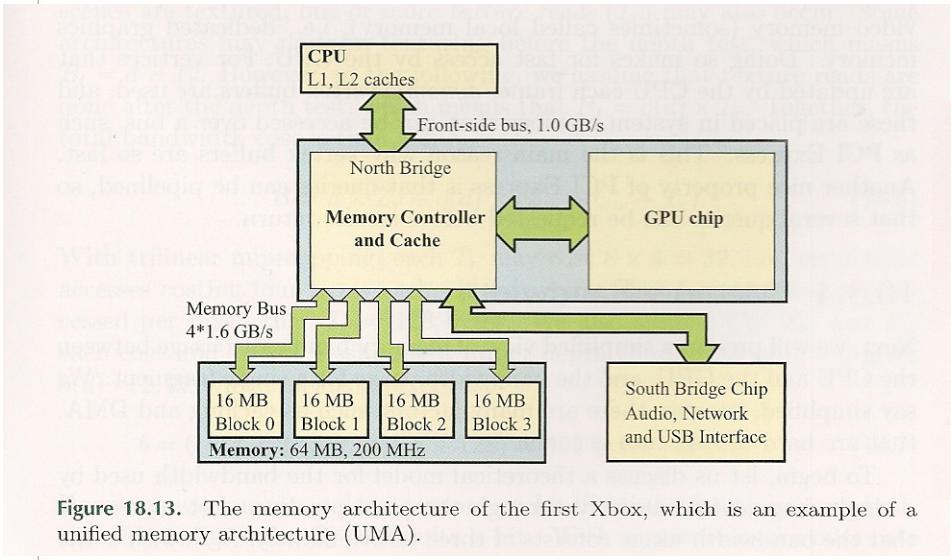
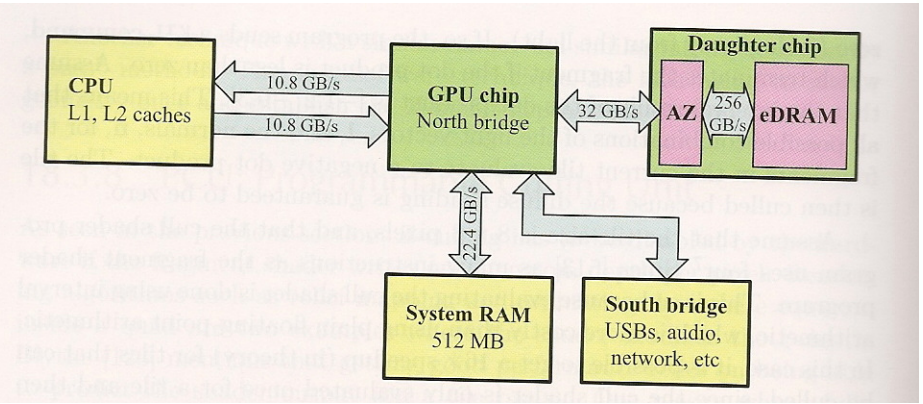


Figure 18.13. The memory architecture of the first Xbox, which is an example of a unified memory architecture (UMA).

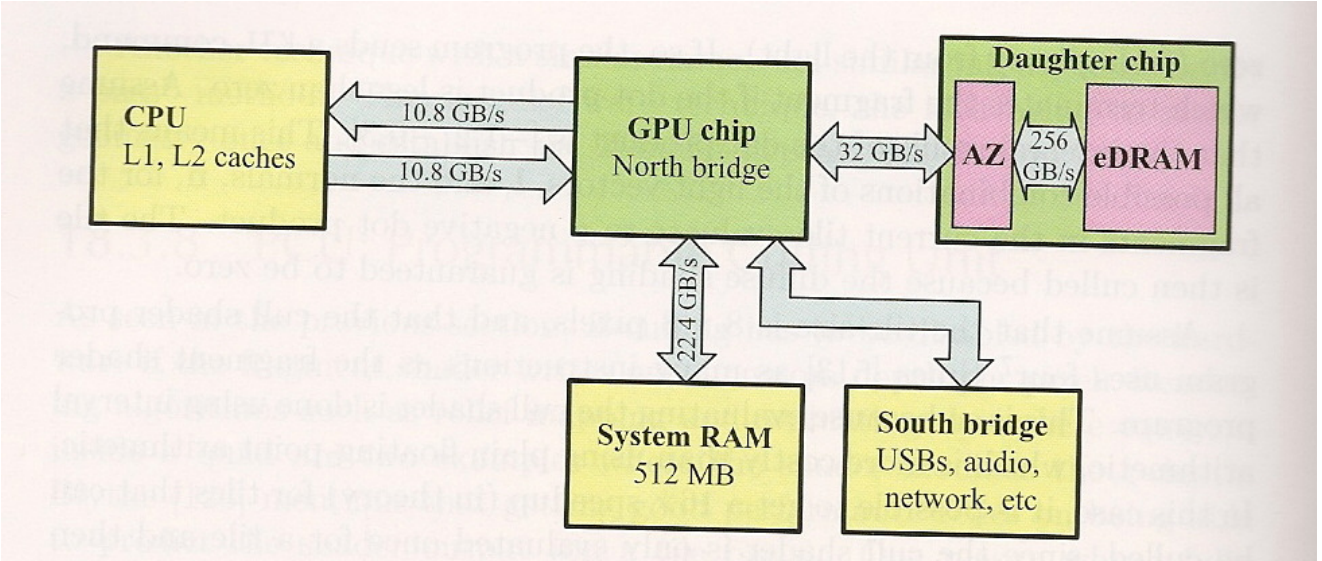




CASE STUDY: XBOX 360

Xbox 360 Memory Architecture

- embedded DRAM(eDRAM): frame buffers,
- 10MB
- Daughter chip: AZ: all alpha and Depth testing.



Xbox 360 System Block Diagram

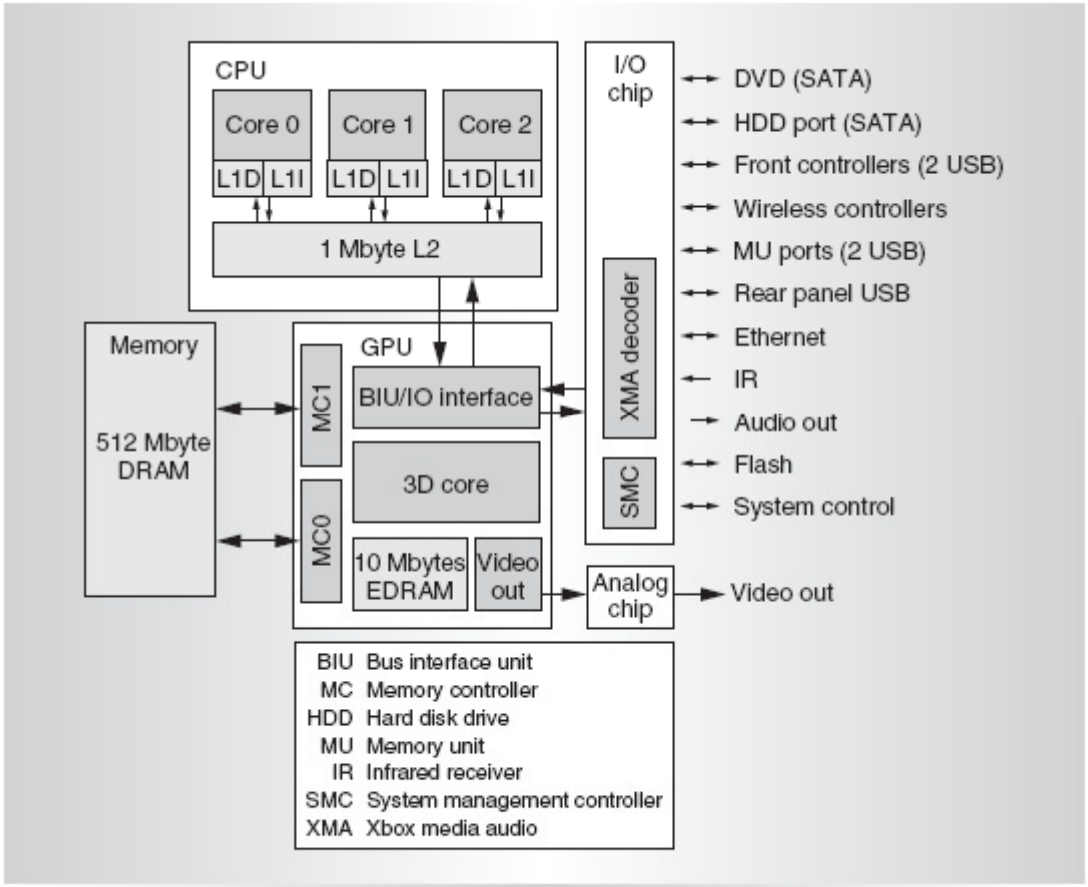


Figure 2. Xbox 360 system block diagram.

Xbox 360 Graphics Processors

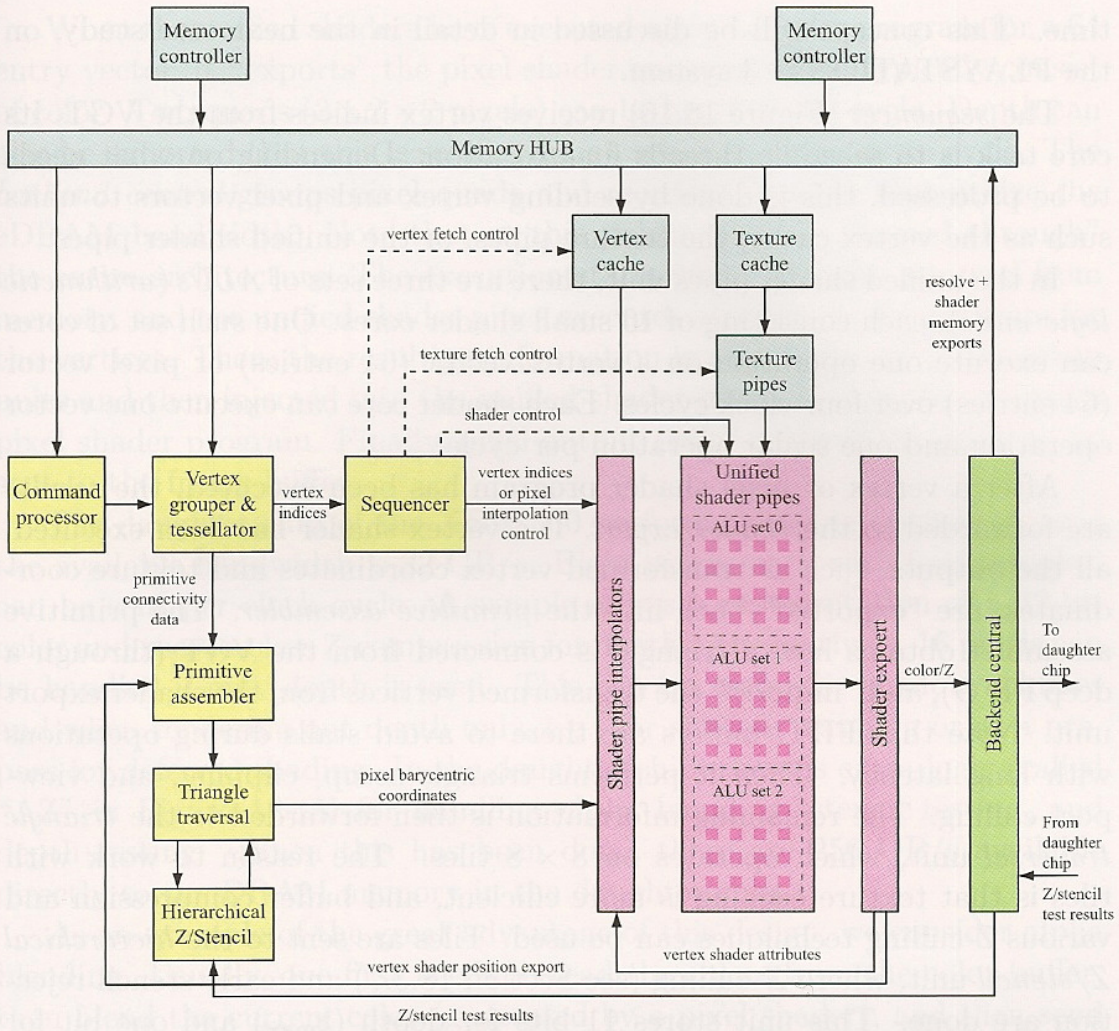


Figure 18.16. Block diagram of the Xbox 360 graphics processor.

Unified shader
Command processor:
reads commands from memory

64 vertices or pixels are operated together (SIMD)

32 vertex threads or 64 pixel threads can be active

24,576 registers

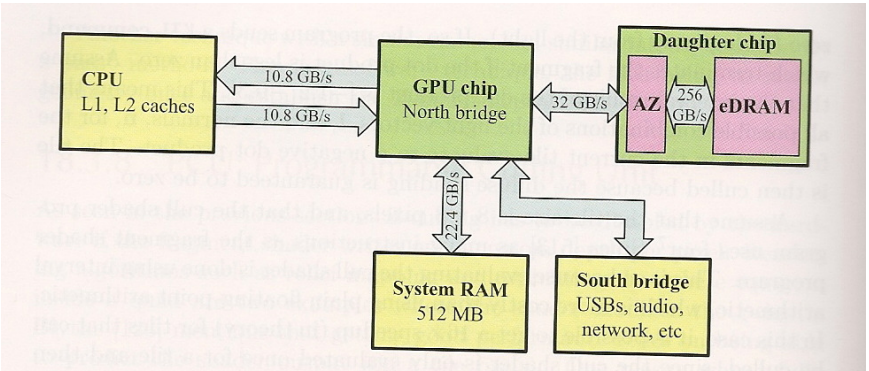
ALI:16 small shader cores
32Kb texture cache
Texture pipes: 16 bilinear filters per cycles



- Command processors: reads commands from memory
- VGT (Vertex grouper & tessellator):
  - Receives a group of vertex indices
- Sequencer: schedule threads
- Shader export: (we need to use the shader again!) FIFO for buffer
- Shader pipe interpolators
- Backend central → send data to daughter chip

Xbox 360 Daughter Chip

- Performs merge operation
- GPU-AZ : bandwidth 32GB/s
- 8 pixels * 4 samples can be sent per clock
  - Sample: 32bit color + lossless z-compression for depth
- 16 pixels if only depth test
- AZ logic: alpha blending, stencil testing, depth testing
- AZ-eDRAM: 256 GB/s



Playstation 3 GPU: The RSX

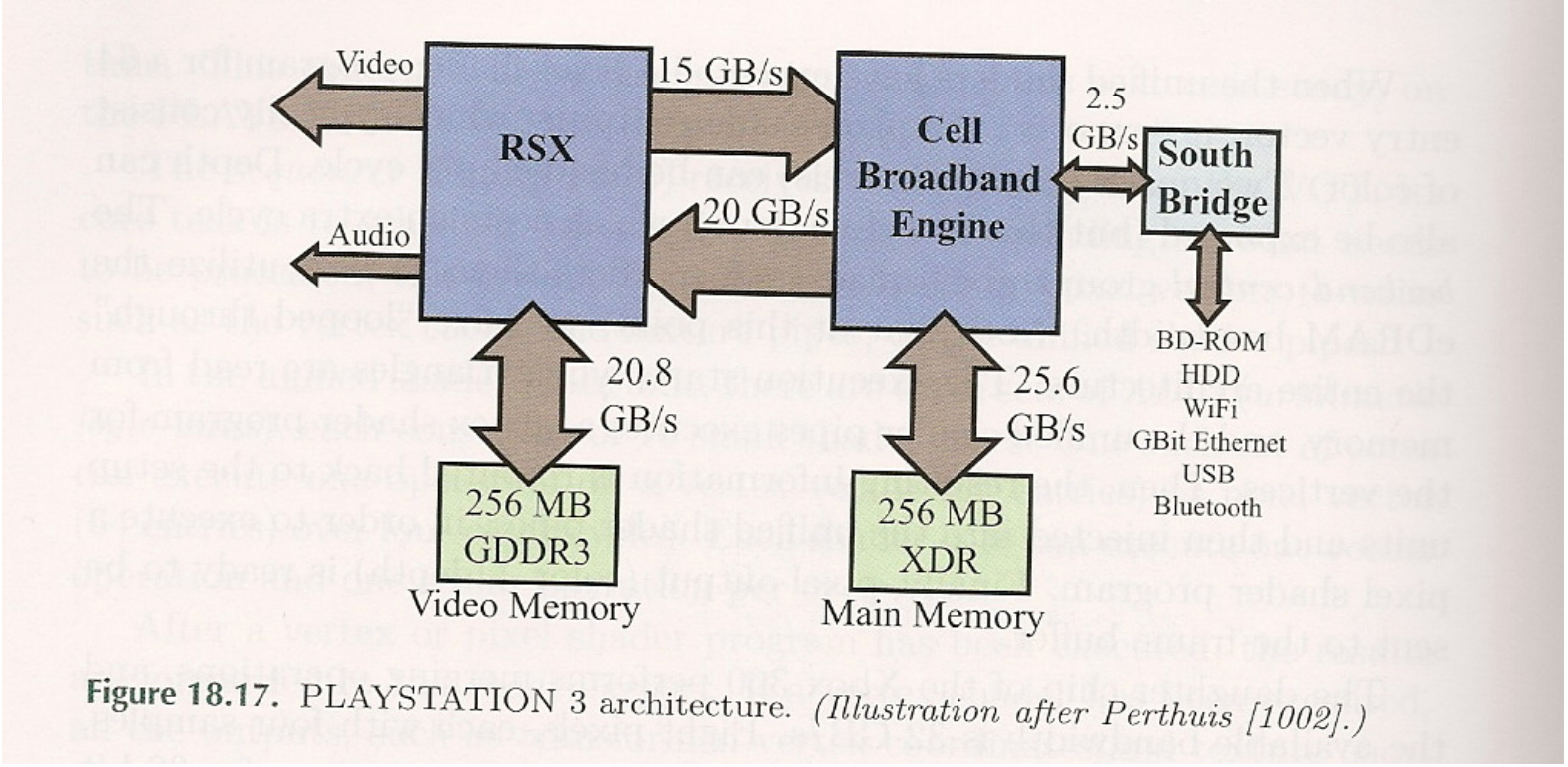


Figure 18.17. PLAYSTATION 3 architecture. *(Illustration after Perthuis [1002].)*

Video memory bandwidth is lower:

Playstation3 GPU Architecture

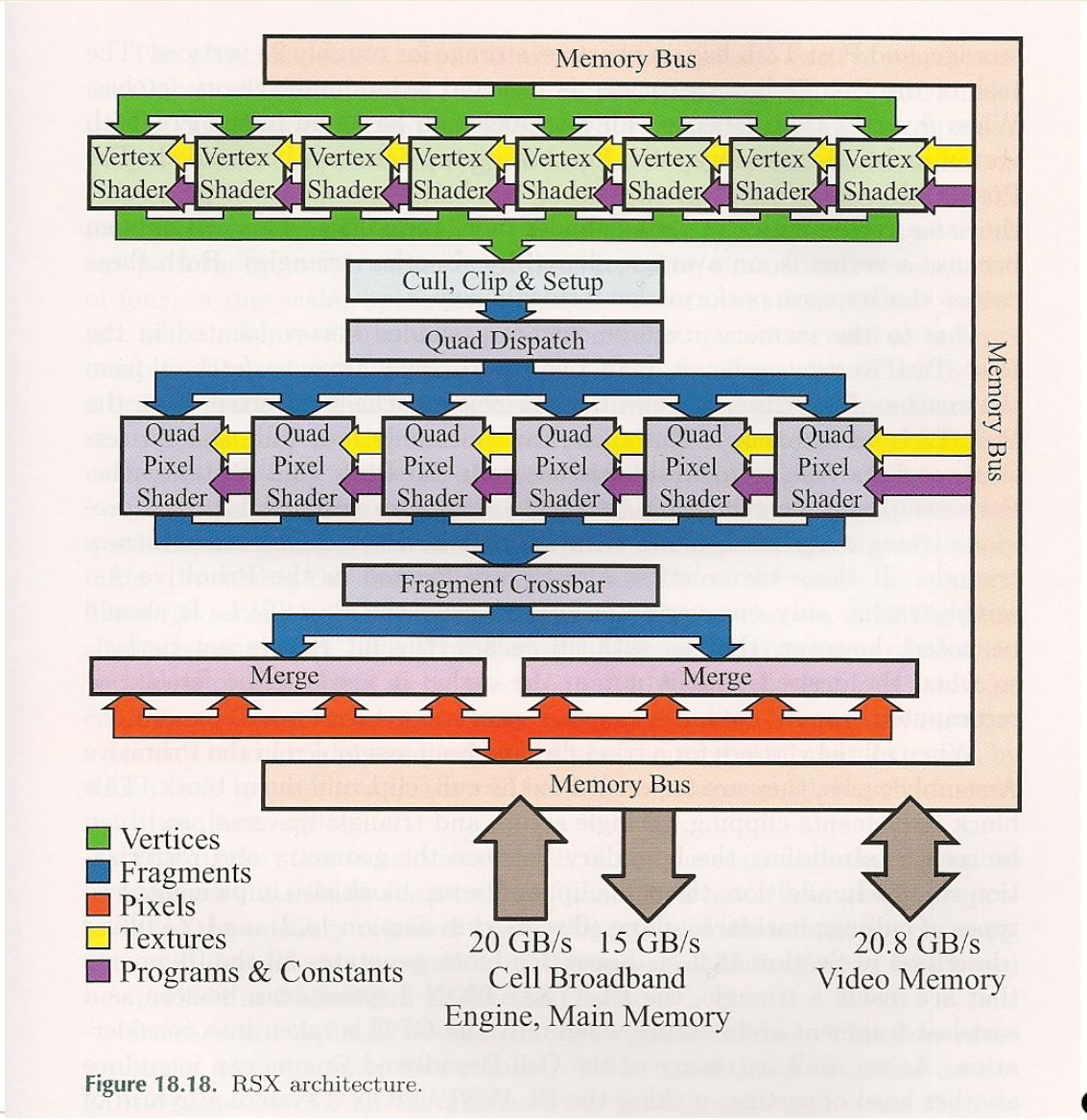


Figure 18.18. RSX architecture.

Modified version of GeForce 7800

8 vertex shader

1 Pre-T&L vertex cache
3 Post- T&L vertex caches

Headsup: Playstaion3 GPU: Cell

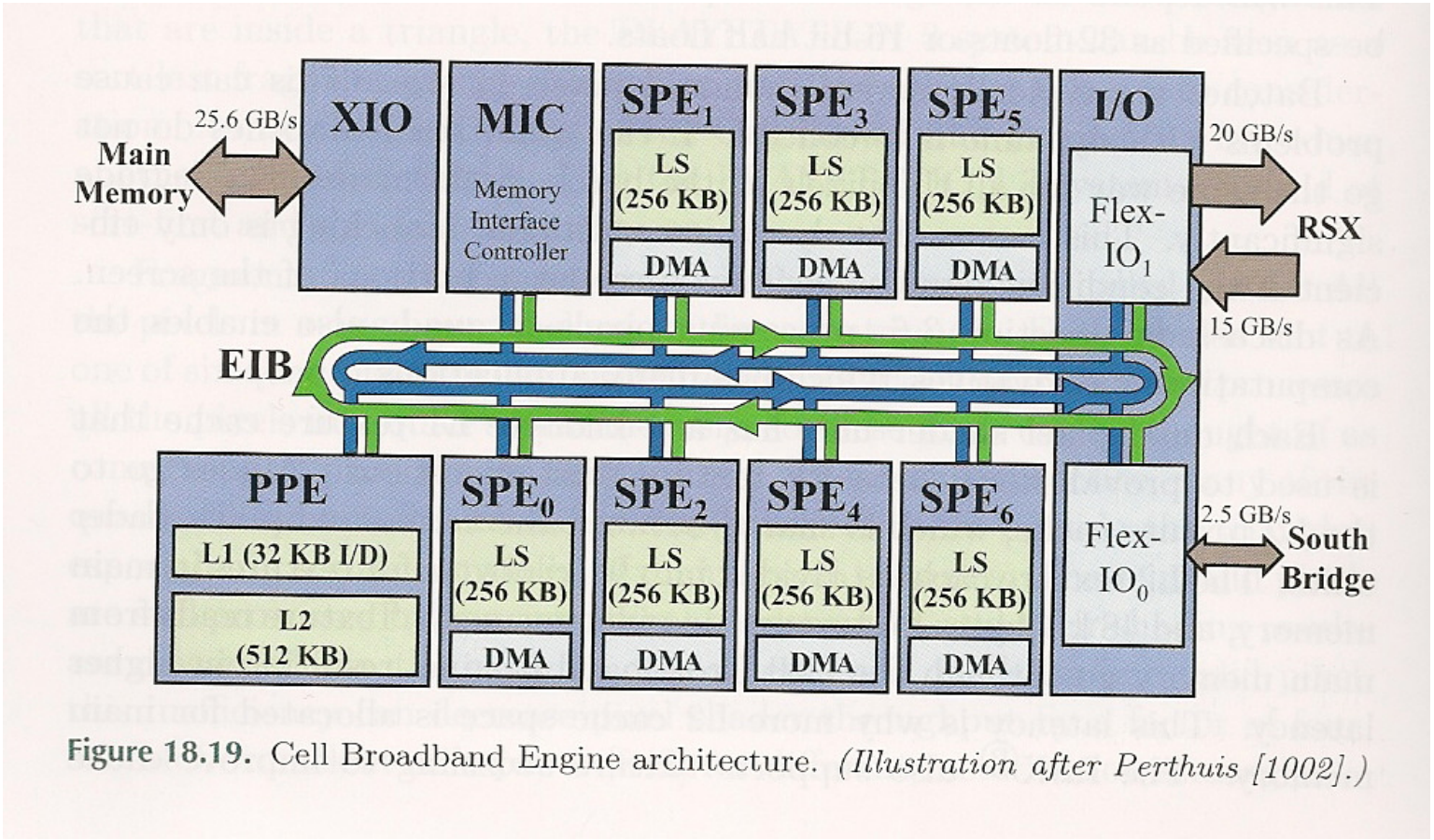


Figure 18.19. Cell Broadband Engine architecture. *(Illustration after Perthuis [1002].)*

Wii's GPU: Hollywood

- Designed by AMD's ATI Technologies
- Almost no public information
  - (no clock frequency, pixel pipelines or shader units)
  - **The 'Hollywood' is a large-scale integrated chip that includes the GPU, DSP, I/O bridge and 3MBs of texture memory," a studio source told us. From Rage3D**
  - Will: Generally more I/O support than peak CPU or GPU performance
- Fixed graphics function.



AMD/ATI

- AMD presentation file (lec_amd.pdf)



Exam Preparation

- Hw#5 :Send the group member list by this Sunday
- Exam material includes discussions in the lectures (beyond the slides)
  - Buzzwords (Xbox360, g80, graphics)
  - G80 architecture questions
  - CUDA programming (general algorithm)